Notice of Allowability	Application No.	Applicant(s)	
	09/902,170	ANDO ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/14/06*.

2. ☒ The allowed claim(s) is/are *1,2,5,7,8,13,14,17,19,20,24,25,28,30,31,50,51,54,56,57,62,63,66,68,69,73,74,77,79 and 80*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *051206* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER

K.N.
May 12, 2006

DETAILED ACTION

Drawings

1. The drawings were received on April 16th, 2004. These drawings are acceptable.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

   Authorization for this examiner's amendment was given in a telephone interview with Mr. Peter A. Veytsman on May 11th, 2006.

3. The application has been amended as follows:

In the Claims:

Cancel dependent claims 3, 15, 26, 52, 64, and 75.

Change claim 1 to -- A method of fabricating a thin film transistor comprising the steps of: providing a gate over a substrate; providing a gate insulating layer over said gate and said substrate; providing an amorphous silicon layer having a first resistance over said gate insulating layer; providing an impurity on the surface of said amorphous silicon layer; forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; subsequently, removing said impurity from said channel region **by exposing said channel region to hydrogen plasma** and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said

contact layer has a second resistance lower than said first resistance; and removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.--.

Change claim 13 to -- A method of fabricating a thin film transistor comprising the steps of: providing a gate over a substrate; providing a gate insulating layer over said gate and said substrate; providing an amorphous silicon layer having a first resistance over said gate insulating layer; providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity; etching said silicon layer utilizing a common photoresist to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; subsequently, removing said impurity from said channel region **by exposing said channel region to hydrogen plasma** and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance; and removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.--.

Change claim 24 to -- A method of fabricating a thin film transistor comprising the steps of: providing a gate over a substrate; providing a gate insulating layer over said gate and said substrate; providing an amorphous silicon layer having a first resistance over said gate insulating layer; providing an impurity on the surface of said amorphous silicon layer; providing a photoresist over said impurity and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate; removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; subsequently, removing said impurity from said channel region **by exposing said channel region to hydrogen plasma** and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein essentially none of said impurity is diffused into said contact portion prior to said removing step; and removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.--.

Change claim 50 to --A method of fabricating a liquid crystal display (LCD) comprising the steps of: providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of: providing a gate over a substrate; providing a gate insulating layer over said gate and said substrate; providing an amorphous silicon layer having a first resistance over said gate insulating layer; providing an impurity on the surface of said amorphous

silicon layer; forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; subsequently, removing said impurity from said channel region **by exposing said channel region to hydrogen plasma** and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.--.

Change claim 62 to --A method of fabricating a liquid crystal display (LCD) comprising the steps of: providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of: providing a gate over a substrate; providing a gate insulating layer over said gate and said substrate; providing an amorphous silicon layer having a first resistance over said gate insulating layer; providing an impurity on the surface of said amorphous silicon layer, wherein said impurity does not diffuse into said amorphous silicon layer; etching said amorphous silicon layer utilizing a common photoresist to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; subsequently, removing said impurity from said channel region **by exposing said channel region to hydrogen plasma** and then diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance; and removing the impurity formed over the amorphous silicon layer in the channel region between the drain and

source electrodes while retaining the impurity over the amorphous silicon layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.--.

Change claim 73 to --A method of fabricating a liquid crystal display (LCD) comprising the steps of: providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of: providing a gate over a substrate; providing a gate insulating layer over said gate and said substrate; providing an amorphous silicon layer having a first resistance over said gate insulating layer; providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity; providing a photoresist over said impurity and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate; removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; subsequently, removing said impurity from said channel region **by exposing said channel region to hydrogen plasma** and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance; and removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.--.

Allowable Subject Matter

4. Claims 1, 2, 5, 7, 8, 13, 14, 17, 19, 20, 24, 25, 28, 30, 31, 50, 51, 54, 56, 57, 62, 63, 66, 68, 69, 73, 74, 77, 79, and 80 are allowed over prior art of record.

Reasons For Allowance

5. The following is an examiner's statement of reasons for allowance:

After further search and consideration of applicants' argument filed on March 14th, 2006, it is determined that the prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach "removing said impurity from said channel region by exposing said channel region to hydrogen plasma" as recited in independent claims 1, 13, 24, 50, 62, and 73.

Claims 2, 5, 7, 8, 14, 17, 19, 20, 25, 28, 30, 31, 51, 54, 56, 57, 63, 66, 68, 69, 74, 77, 79, and 80 are also allowed as being directly or indirectly dependent of the allowed independent base claims.

Conclusion

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US-6,624,051	09-2003	Ohtani et al.
US-6,444,508	09-2002	Tanabe et al.
US-6,214,684	04-2001	Shoji, Tatsumi
US-5,990,489	11-1999	Tashiro, Kazuaki

US-5,637,512	06-1997	Miyasaka et al.
US-5,591,989	01-1997	Miyasaka et al.

These references are related to method of fabricating thin film transistor but does not teach or suggest "removing said impurity from said channel region by exposing said channel region to hydrogen plasma" as recited in independent claims 1, 13, 24, 50, 62, and 73.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
May 12, 2006

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER